Amendments to the Drawings:

Replace Fig. 2 and Fig. 3 with the attached Fig. 2 and Fig. 3.

REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1, 2, and 4-28 are pending in this case. Claims 1, 4, and 10 are amended herein and claims 3 and 29-44 are cancelled herein.

The Examiner objected to the drawings as Figs. 1-3 use the same reference numerals to refer to different structures. Both overlap capacitances 124 and 126 and a layer of dielectric material 124 and gate electrode layer 126 are shown. Replacement sheets 1 and 2 amend Figs 2 and 3 by illustrating the layer of dielectric material as 108 and the gate electrode layer as 106.

The Examiner similarly objected to the specification. The specification is amended herein to refer to the layer of dielectric material 108 and gate electrode layer 106. The overlap capacitances continue to be referred to as 124 and 126.

The Examiner objected to claims 3-10, 14, 20, and 22-26 as being dependent upon a rejected base claim but that would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 3 is rewritten as amended claim 1 including all the limitations of the base claim, former claim 1. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are allowable.

The Examiner rejected claims 1, 2, 15 and 21 under 35 U.S.C. 102(e) as being anticipated by Dokumaci et al. (U.S. Patent 6,686,637).

Applicant respectfully submits that amended claim 1 and the claims dependent thereon are unanticipated by Dokumaci for the reasons discussed above relative to claim 3 whose limitations have been incorporated into claim 1.

Applicant respectfully submits that claim 15 is unanticipated by Dokumaci as there is no disclosure or suggestion in the reference of patterning the poly-Si, poly-SiGe with carbon and dielectric layers to form a gate stack as required by claim 15. Dokumaci teaches forming a poly-Si block 102, forming an oxide layer 108, recessing the poly-Si block to form poly-Si region 110, forming a barrier 112, forming a second poly-Si layer 116, then planarizing layers 116 and 112, and finally removing oxide 108. While the original poly-Si block 102 may be patterned and etched in Dokumaci, patterning is not used on all of the poly-Si, poly-SiGe, and dielectric layers to form a gate stack, as required by the claim. Instead of patterning, Dokumaci deposits the barrier and second poly-Si layer in recess 114 and planarizes these layers to form a gate stack (along with removing the oxide 108). Accordingly, Applicant respectfully submit that claim 15 and the claims dependent thereon are unanticipated by Dokumaci.

The Examiner rejected claims 11-12 and 27-28 under 35 U.S.C. 103(a) as being unpatentable over Dokumaci et al. (U.S. Patent 6,686,637) in view of Sagnes (U.S. Patent 5,998,289).

Applicant respectfully submits that claims 11 and 12 are patentable over the references due to the amendment of claim 1, from which these claims depend, incorporating the limitations of claim 3.

Applicant respectfully submits that claims 27 and 28 are patentable over the reference as there is no disclosure or suggestion in the references of patterning the poly-Si, poly-SiGe with carbon and dielectric layers to form a gate stack as required by claim 15, from which these claims depend. As discussed above, Dokumaci fails to disclose or suggest this limitation. Sagnes is added to teach thicknesses of various layers.

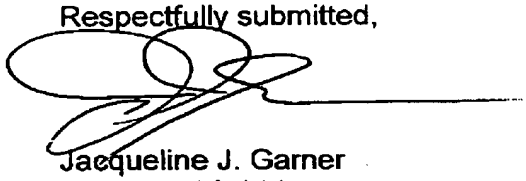
The Examiner rejected claims 13, and 16-19 under 35 U.S.C. 103(a) as being unpatentable over Dokumaci et al. (U.S. Patent 6,686,637) in view of Moslehi (U.S. Patent 5,397,909).

Applicant respectfully submits that claim 13 is patentable over the references due to the amendment of claim 1, from which claim 13 depends, incorporating the limitations of claim 3.

Applicant respectfully submits that claims 16-19 are patentable over the reference as there is no disclosure or suggestion in the references of patterning the poly-Si, poly-SiGe with carbon and dielectric layers to form a gate stack as required by claim 15, from which these claims depend. As discussed above, Dokumaci fails to disclose or suggest this limitation. Moslehi likewise fails to teach this limitation.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1, 2, and 4-28. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



Jacqueline J. Garner
Reg. No. 36,144

Texas Instruments Incorporated
P. O. Box 655474, M.S. 3999
Dallas, Texas 75265
Phone: (214) 532-9348
Fax: (972) 917-4418